an epitaxial (EPI) layer over the substrate region, wherein the plurality of device structures are provided in the EPI layer.

26. (Amended) The high current interconnect of claim 25 wherein the plurality of metals comprises two metals, a first metal covers one-half of the slot and a second metal fills the slot.

IN THE ABSTRACT

Please replace the Abstract, beginning on page 29, line 2, with the following Abstract:

A method and system for providing an interconnect on a semiconductor device is disclosed. The method and system comprises providing a semiconductor substrate with a plurality of device structures thereon and providing at least one slot in the semiconductor substrate. The method and system include providing a metal within the at least one slot.

This first metal in a preferred embodiment consists of three depositions of metal when sputtered, with the first two depositions being buried in the silicon prior to a dielectric and a third deposition of what is called the first metal layer. This third deposition provides the normal interconnect pattern as it normally is patterned in standard metalization schemes.